Dr. CU 2.0: A Scalable Detailed Routing Framework with Correct-by-Construction Design Rule Satisfaction*

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*Source code is available at https://github.com/cuhk-eda/dr-cu.

Outline

Outline

Detailed Routing

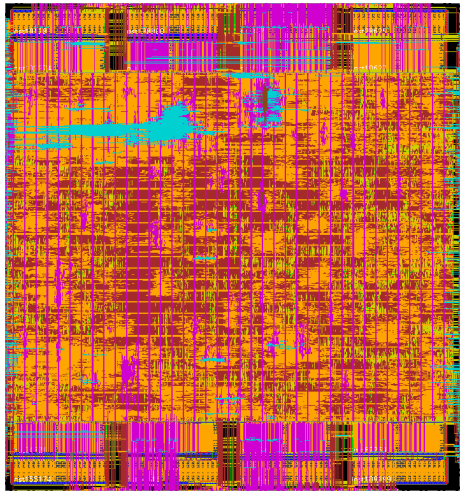


Figure 1: Quad-Core Design [Liu et al. 2019].

- 1M nets in $20\text{K} \times 20\text{K} \times 10$ grid points, hardly routed by ILP-based [a] or SAT-based [b] methods.
- Complicated design rules:
  - Parallel run length (PRL) spacing [c].
  - End-of-line (EOL) spacing.
  - EOL spacing with parallel edges [d].
  - Corner-to-corner (C2C) spacing [e].

[a] [Kahng, Wang, and Xu 2018]
[b] [Park et al. 2019]
[c] [Qi, Cai, and Zhou 2015]
[d] [Yu et al. 2015]
[e] [Côté, Pierrat, and Hurat 2004]

Problem Formulation

Given

- technology node and design rules,
- placement result with netlist,
- routing tracks and blockages, and
- route guides generated from global routing,

route all nets minimizing a weighted sum of

- total wire-length and via count,
- out-of-guide, off-track, wrong-way usage, and
- design rule violations.

Contributions

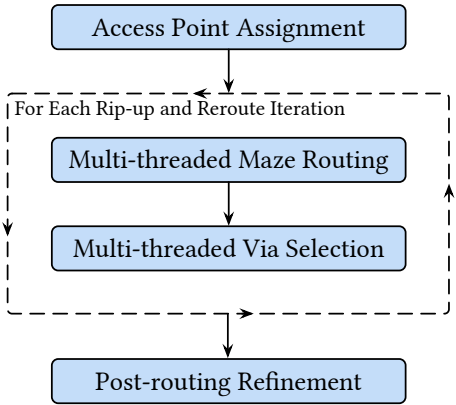


Figure 2: Detailed Routing Flow.

- Compute valid access points of each pin and create off-track vias if no same-layer access point is valid.
- Handle end-of-line spacing with parallel edges in a correct-by-construction manner.
- Fix corner-to-corner spacing violations in post-processing.
- Develop a lookup-table-based via insertion method and select violation-free via types from the cell library.

Outline

Two-Level Sparse Data Structures

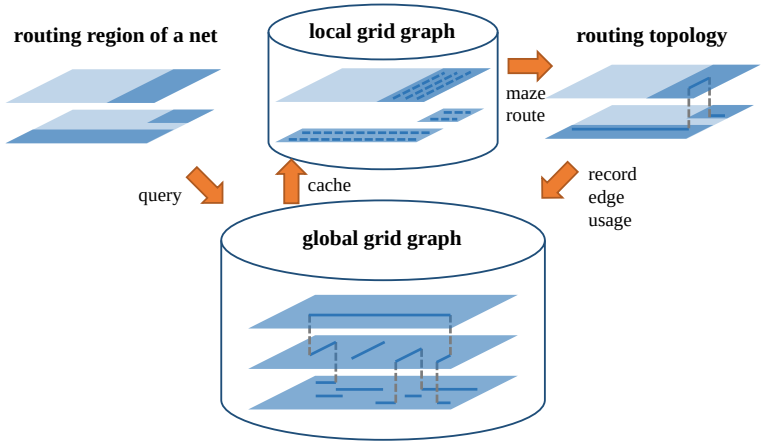


Figure 3: Global and Local Grid Graph.

Parallel Run Length Spacing

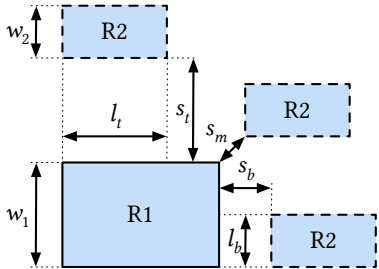


Figure 4: Parallel Run Length Spacing.

The parallel run length (PRL) spacing requirements between two wires of different nets depend on both width and PRL of the two wires.

End-of-line Spacing

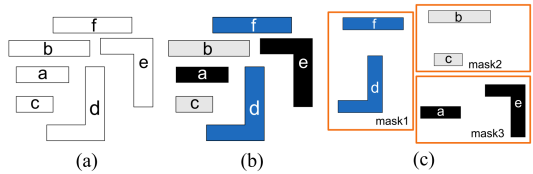


Figure 5: Example of Triple Patterning Layout Decomposition †.

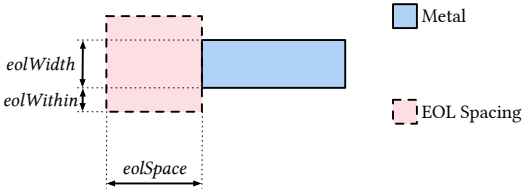


Figure 6: EOL Spacing without Parallel Edges.

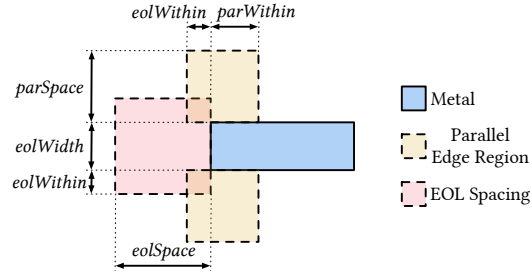


Figure 7: EOL Spacing with Parallel Edges.

†[Yu et al. 2015]

Corner-to-Corner Spacing

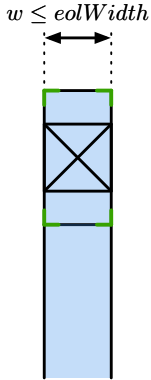


Figure 8: C2C spacing does not apply.

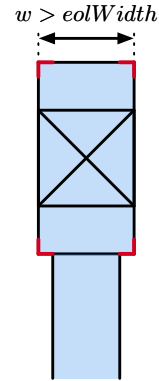
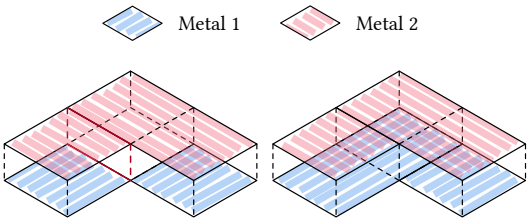


Figure 9: C2C spacing applies.

Outline

Local Grid Graph Construction



(a) Before Expansion. (b) After Expansion.

Figure 10: Unconnected Route Guides.

- Expand route guides in preferred routing direction for full connections.
- Expand in x- and y-direction for each rip-up-and-reroute iteration.
- Extend to adjacent layers if the numbers of violations exceed a threshold.

Pin Access

- Assign same-layer surrounding grid points as access points by default.
- Use diff-layer access points by an off-track via if no valid same-layer access points.
- Penalize other nets for using grid points above/below it before it is connected.

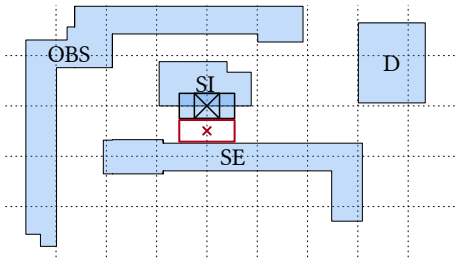


Figure 11: No valid same-layer access point.

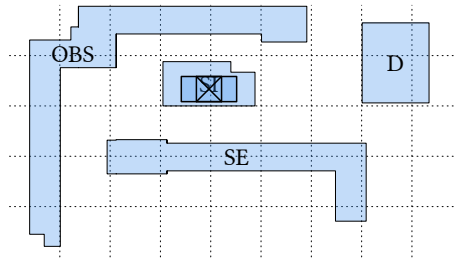


Figure 12: Use off-track via

Via Type Selection Flow

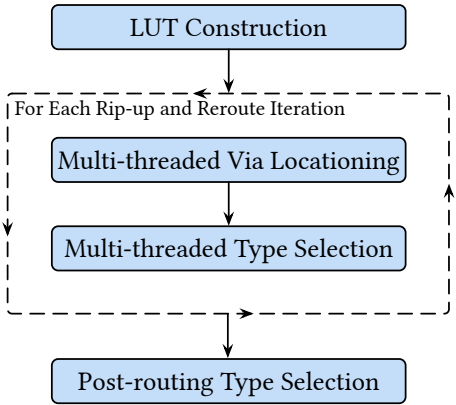


Figure 13: Detailed Routing Flow.

- Construct via conflict lookup tables (LUTs).
- Determine via locations and generate routing topology for a net.
- Perform via type selection for the net.
- Finally decide via type globally in a post refinement stage.

Via Conflict Lookup Table

- Via-pin/obstacle conflicts.
- Via-wire conflicts.
- Via-via conflicts.

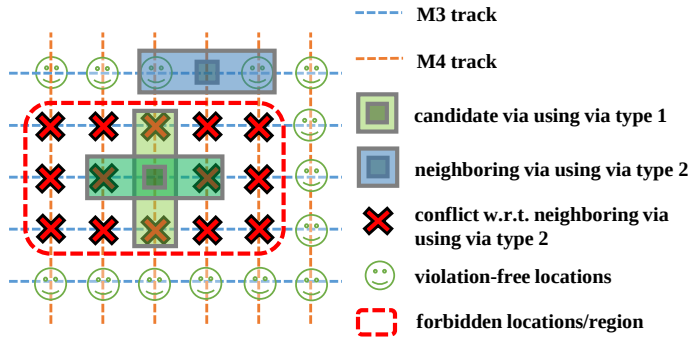


Figure 14: Via-via LUT.

Pessimistic Lookup Table

- Checking every via-type during routing is time-consuming.
- Merged LUTs records all suspicious conflicts.
- Suspicious conflicts can be verified when the via types are determined.

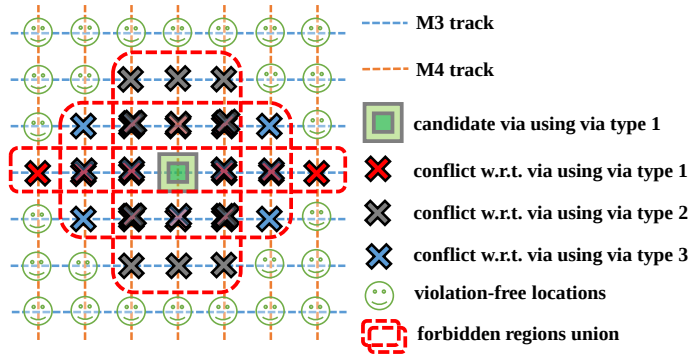


Figure 15: Merged Via-via LUT.

Parallel Run Length Spacing Handling

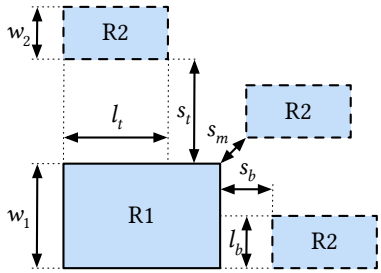


Figure 16: Parallel Run Length Spacing.

Figure 17: Spacing Table

		Parallel Run Length				
		0.00	0.22	0.47	0.63	1.50
Width	0.00	0.05	0.05	0.05	0.05	0.05
	0.09	0.05	0.06	0.06	0.06	0.06
	0.16	0.05	0.10	0.10	0.10	0.10
	0.47	0.05	0.10	0.13	0.13	0.13
	0.63	0.05	0.10	0.13	0.15	0.15
	1.50	0.05	0.10	0.13	0.15	0.50

Penalize some tracks along power and ground rails.

End-of-line Spacing Handling

Assume that a parallel edge exist to avoid blocking neighboring tracks.

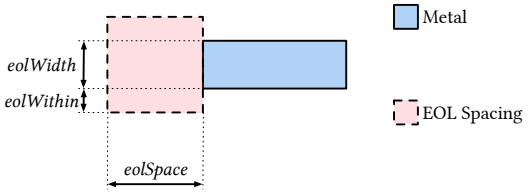


Figure 18: EOL Spacing without Parallel Edges.

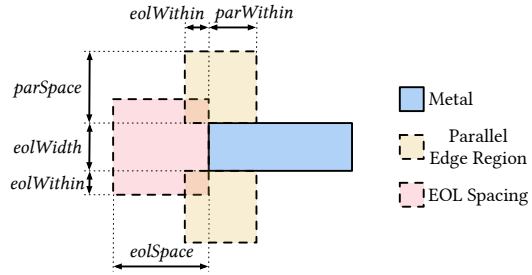


Figure 19: EOL Spacing with Parallel Edges.

Corner-to-Corner Spacing Handling

Slightly extend an on-track wire segment that connects a wrong-way wire segment.

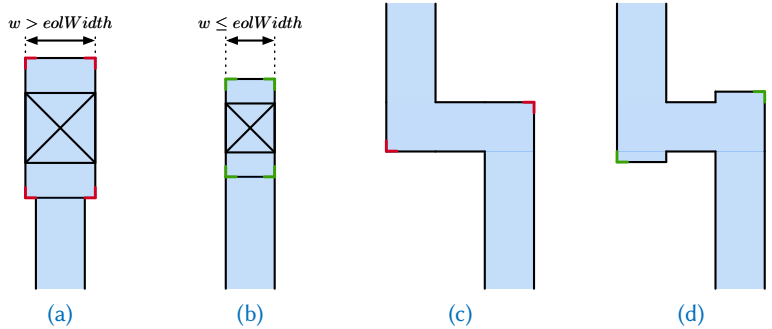
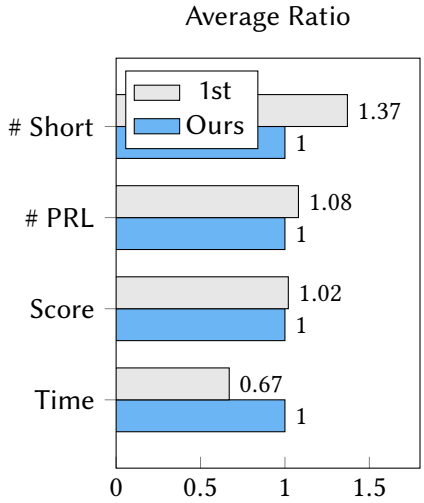
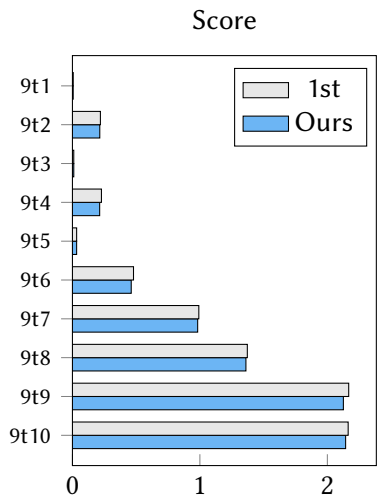


Figure 20: (a) Via applied to C2C. (b) Via not applied to C2C. (c) Wrong-way wire applied to C2C. (d) Wrong-way wire not applied to C2C.

Outline

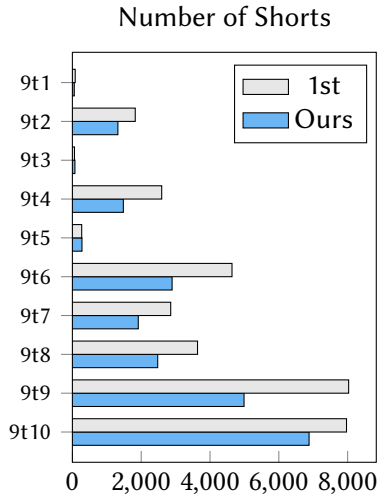
Comparison with 1st in ISPD 2019 Contest ‡

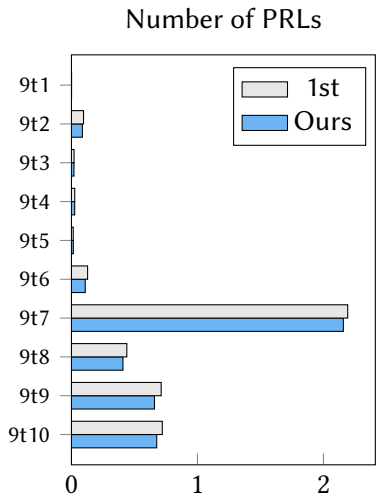




‡[Liu et al. 2019]

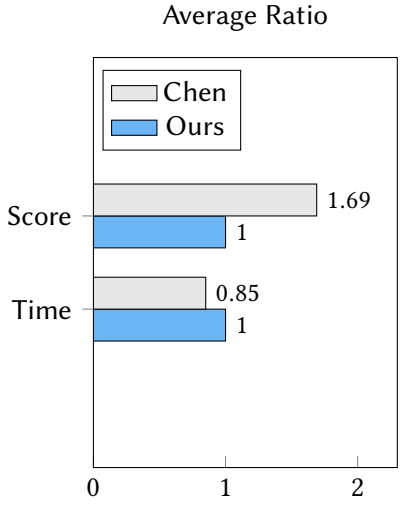
Comparison with 1st in ISPD 2019 Contest §

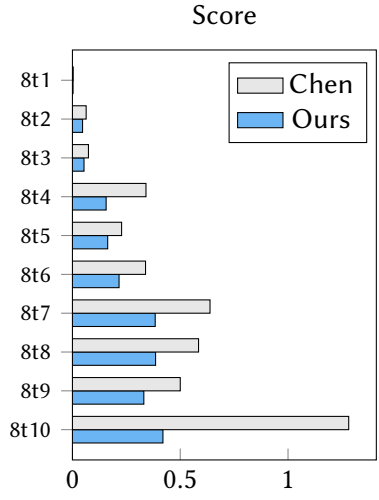




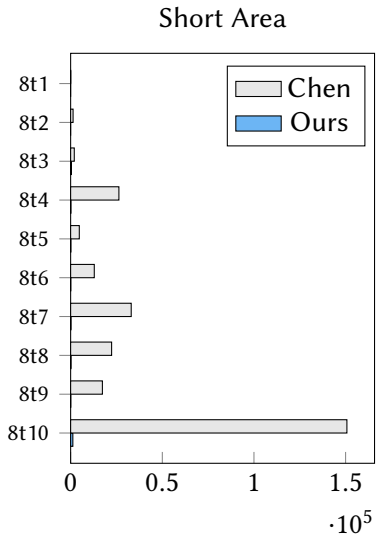
§[Liu et al. 2019]

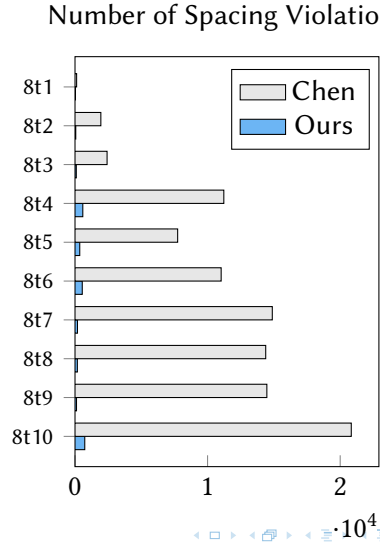
Comparison with [Chen et al. 2019]



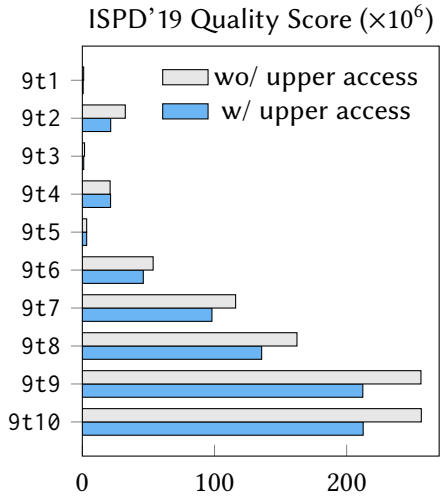


Comparison with [Chen et al. 2019]

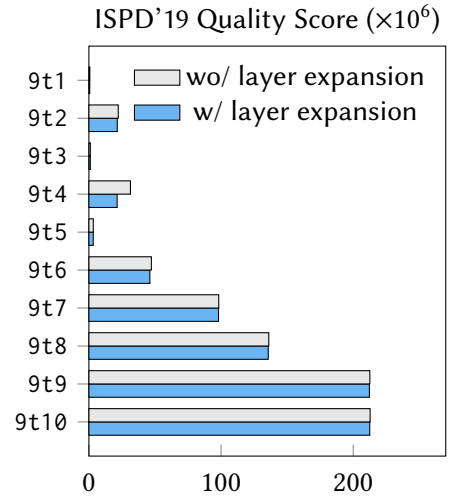




Comparison between Different Settings



(a) Upper-layer Access Points with Off-track Vias.



(b) Layer Expansion of Local Grid Graphs.

Outline

Conclusion

- Compute valid access points of each pin and create off-track vias.
- Handle end-of-line spacing with parallel edges during routing.
- Fix corner-to-corner spacing violations in post-processing.
- Develop a lookup-table-based via insertion method.

Thanks!

Questions?

References I

- Chen, Gengjie, Chak-Wa Pui, Haocheng Li, Jingsong Chen, Bentian Jiang, and Evangeline FY Young (2019). "Detailed routing by sparse grid graph and minimum-area-captured path search". In: *Proceedings of the 24th Asia and South Pacific Design Automation Conference*. ACM, pp. 754–760.
- Côté, Michel Luc, Christophe Pierrat, and Philippe Hurat (Oct. 2004). *Accelerated layout processing using OPC pre-processing*. US Patent 6,807,663.
- Kahng, Andrew B, Lutong Wang, and Bangqi Xu (2018). "TritonRoute: an initial detailed router for advanced VLSI technologies". In: *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*. IEEE, pp. 1–8.
- Liu, Wen-Hao, Stefanus Mantik, Wing-Kai Chow, Yixiao Ding, Amin Farshidi, and Gracieli Posser (2019). "ISPD 2019 Initial Detailed Routing Contest and Benchmark with Advanced Routing Rules". In: *Proceedings of the 2019 International Symposium on Physical Design*. ACM, pp. 147–151.

References II

- Park, Dongwon, Ilgweon Kang, Yeseong Kim, Sicun Gao, Bill Lin, and Chung-Kuan Cheng (2019). “ROAD: Routability Analysis and Diagnosis Framework Based on SAT Techniques.”. In: *ACM International Symposium on Physical Design (ISPD)*, pp. 65–72.
- Qi, Zhong-Dong, Yi-Ci Cai, and Qiang Zhou (2015). “Design-Rule-Aware Congestion Model with Explicit Modeling of Vias and Local Pin Access Paths”. In: *Journal of Computer Science and Technology* 30.3, pp. 614–628.
- Yu, Bei, Kun Yuan, Duo Ding, and David Z. Pan (Mar. 2015). “Layout Decomposition for Triple Patterning Lithography”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* 34.3, pp. 433–446.